Thesys-Intechna

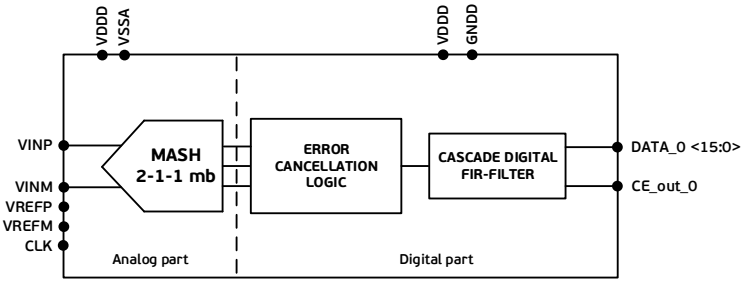
16-bit delta-sigma ADC, 1 MSPS

DATA SHEET TI-16DS

FEATURES

- 16-bit resolution
- Sample rate: 1 MSPS
- Clock frequency: 32 MHz
- Differential input range 2.4 V-V
- INL: ± 2 LSB
- DNL: ± 1 LSB
- Effective number of bits: 14.5 bits
- Operating temperature range: -40°C..+110°C

FUNCTIONAL BLOCK DIAGRAM



HIGHLIGHTS

- Fully differential architecture
- Input signal bandwidth: 500 kHz
- Linear phase response
- MASH architecture
- Parallel digital output

APPLICATIONS

- Medical equipment
- Precision Industrial Measurements
- Local Networks

GENERAL DESCRIPTION

The TI-16DS is a high-speed, precision 16-bit delta-sigma ADC with a fully differential architecture and a 500 kHz bandwidth. Oversampling, which is based on the operation of this ADC, makes it possible to reduce the sensitivity to the phase jitter of a clock signal during the sampling of a high-frequency signal with a large amplitude.

The digital part consists of a digital error correction block and a digital cascade FIR filter with linear phase response.

LIST OF CONTENTS

DEVICE PARAMETERS

VDDA = 3.3 V; VDDD = 1.62..1.98 V; dVREF=1.2 V; VCM = 1.65 V; F_{CLK} = 32 MHz; T = -40..110 ^{0}C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit	Conditions and comments
Accuracy						
N	Resolution		16		Bits	
INL	Integral nonlinearity			±2	EMP	Fin = 167 kHz sine wave; Fclk = 32 MHz
DNL	Differential nonlinearity			±1	EMP	
Dynamic parameters						
ENOB	Effective number of bits			14.54	Bits	Fin = 167 kHz sine wave; Fclk =32 MHz
SNR	Signal-to-Noise ratio			90.57	dB	
SINAD	Signal-to-Noise and distortion ratio			89.33	dB	
THD	Total Harmonic Distortion			-95.35	dB	
Reference inputs						
dVREF	Low reference level			1.2	V	
VCM	Common mode voltage		1.65		V	
Digital inputs						
V_{IH}	Input high voltage level	1.4			V	
V_{IL}	Input low voltage level			0.4	V	
C_{IND}	Input capacitance			96	fF	
V_{OH}	Output high voltage level			VDDD	V	
V_{OL}	Output low voltage level	0			V	
C_L	Load capacitance	500			fF	Rising/falling edge is 2 ns
Current consumption						
Idda	Analog part			22.77	mA	F_{clk} = 32 MHz
Iddd	Digital part			6.27	mA	
Timing						
F_{CLK}	Clock frequency			32	MHz	

PIN FUNCTIONAL DESCRIPTION

Pin name	Description	Comments
nRST	Reset ADC	Active level – low Asynchronous
CLK	Clock input	
EN	Clock enable	Active level - high
VDDD	Digital power supply	Typical value: 1.8 V
GNDD	Digital ground	
VDDF	Clock module power supply	Typical value: 3.3 V
VSSF	Clock module ground	
VDDA	Analog power supply	Typical value: 3.3 V
VSSA	Analog ground	
VREFP	High reference voltage	
VREFM	Low reference voltage	
VCM	Common-mode voltage	
VINP	Analog input (+)	
VINM	Analog input (-)	
DATA_O <15:0>	Digital output data <15:0>	
CE_OUT_O	Output enable	
EN_IEXT	Enable external current source	Active level - high, disables internal biasing
IEXT	External current input	
B <3:0>	Internal current source control	
SHIELD	Shield (ground)	
PSUB	Substrate potential	

TIMING DIAGRAM

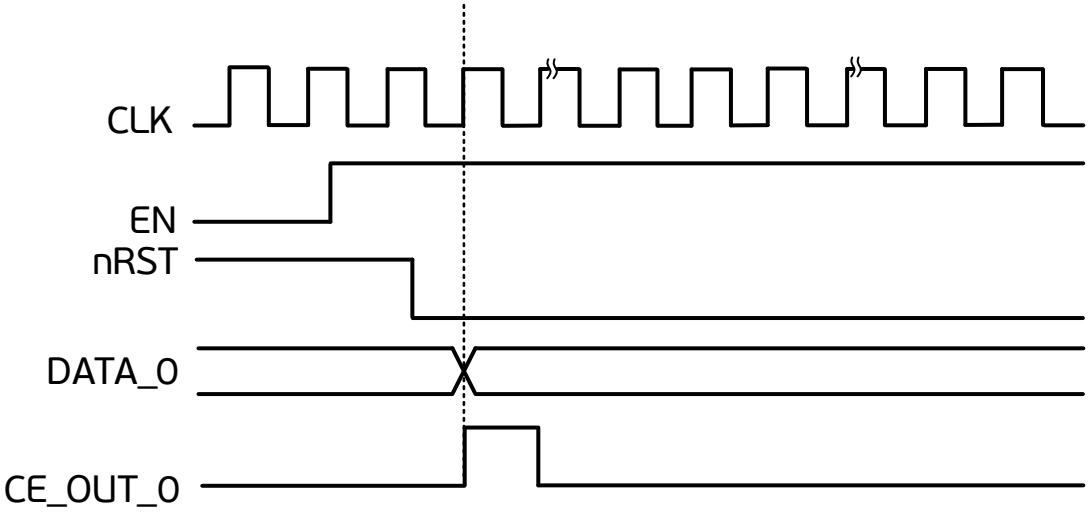


Figure 1. Timing diagram

The digital part is reset by the high level nRST. CE_OUT_O is responsible for the availability of digital data. Reading data DATA_OUT_O is recommended by the fall of CE_OUT_O.

INTERNAL CURRENT SOURCE

The implemented current source is a general-purpose current source. It is powered by VDDA and is controlled by B<3:0>.

Internal current source output current (VDDA = 3.3 B, T = 27 °C)

Code	Output current, uA
B<3:0>=0000	38.08
B<3:0>=0001	59.24
B<3:0>=0010	80.39
B<3:0>=0100	101.54
B<3:0>=1000	122.7
B<3:0>=1001	143.85
B<3:0>=1111	249.4

REQUIREMENTS FOR POWER SUPPLY AND GROUND NETS

Analog and digital power supplies wiring should be split, because the analog blocks require isolation from digital power supply noise.