Thesys-Intechna

# 12-bit Pipeline ADC, 20 MSPS

DATA SHEET TI-12PI/20M

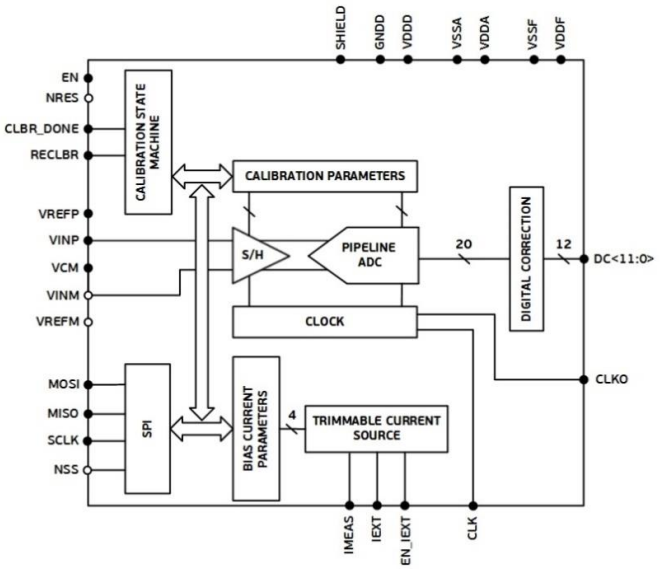
## FEATURES

- 12-bit resolution
- Sample rate: 20 MSPS
- INL: ±3 LSB
- DNL: ±0.8 LSB
- ENOB at 1.3 MHz input: 10.1 bits

## HIGHLIGHTS

- Fully differential architecture
- Integrated/external biasing choice
- Trimming mode of internal biasing
- Built-in calibration state machine for offset and gain calibration
- Built-in SPI for parameters tuning including Speed-to-Power Consumption ratio trimming
- Output clock for output data processing
- Separate analog and digital power supplies (5 V and 1.8 V correspondingly)

## FUNCTIONAL BLOCK DIAGRAM




## APPLICATIONS

- Space applications
- Communications
- SDR receivers
- Test and instrumentation

## GENERAL DESCRIPTION

The TI-12PI/20M is a 12-bit analog-to-digital converter (ADC) with pipelined architecture and serial peripheral interface (SPI), which achieves conversion rate up to 20 MSPS. It has differential analog inputs and parallel data output. The device includes internal Sample & Hold (S&H) circuit, eight 1.5-bit stages, and one 4-bit Flash AD converter. Internal automatic prestart calibration system allows to tune consequently offset and gain of each pipeline stage using built-in analog calibration arrays for each parameter. Consequent calibration approach results in high static and dynamic parameters of the whole pipeline ADC system. The calibration module can be activated by power-on or by user. The SPI allows user to configure the following ADC parameters: biasing current, calibration coefficients of each stage, number of calibration iterations, delay between offset and gain calibrations.

User can make speed adjustment of operational amplifiers and comparators by adjusting internal current source or by using external current source for biasing. To increase speed, current should also be increased, but power consumption in this case rises as well. Thus, speed-to-power consumption ratio trimming is available.

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## DEVICE PARAMETERS

VDDA = 4.5 to 5.5 V, VDDD = 1.62 to 1.98 V, VSSA = GNDD = 0 V; VREFP = VDDA, VREFM = 0, VCM = 0.5*VDDA, $F_{CLK}$ = 20 MHz, internal $I_{BIAS}$ with default value (8), calibrated with internal routing, T = −40 to 150°C, unless otherwise noted

| Symbol | Parameter | Min | Typ | Max | Unit | Conditions and comments |
|---|---|---|---|---|---|---|
| Accuracy [A] | | | | | | |
| N | Resolution | | 12 | | Bits | |
| INL | Integral nonlinearity | | ±3.15 | ±3.31 | LSB | $F_{in}$ = 1.3 MHz sine wave; $F_{CLK}$ = 20 MHz |
| DNL | Differential nonlinearity | | ±0.86 | ±1.06 | LSB | |
| OE | Offset error | | ±0.68 | ±2.38 | LSB | |
| GE | Gain error | | 0.99 | 1.00 | % | |
| Dynamic parameters [A] | | | | | | |
| ENOB | Effective number of bits | 9.26 | 9.93 | 10.10 | Bits | $F_{in}$ = 1.3 MHz sine wave; $F_{CLK}$ = 20 MHz |
| SNR | Signal-to-Noise ratio | 59.9 | 62.5 | 63.6 | dB | |
| SINAD | Signal-to-Noise and distortion ratio | 57.5 | 61.5 | 62.5 | dB | |
| SFDR | Spurious-Free Dynamic Range | 61.9 | 68.8 | 70.75 | dB | |
| THD | Total Harmonic Distortion | 0.3 | 0.4 | 0.8 | m% | |
| Reference inputs | | | | | | |
| VREFP | High reference voltage | VCM+2 | | VDDA | V | |
| VREFM | Low reference voltage | VSSA | | VCM-2 | V | |
| VCM | Common mode voltage | 2 | 2.5 | 3 | V | |
| $C_{REFP}$ | VREFP input capacitance | | 15.4 | | pF | |
| $C_{REFM}$ | VREFM input capacitance | | 17.7 | | pF | |
| $C_{CM}$ | VCM input capacitance | | 3.6 | | pF | |
| Irefp | Current through VREFP [A] | 1.95 | 2.44 | 4.04 | mA | Sourcing, dynamic |
| Irefm | Current through VREFM [A] | 1.95 | 2.44 | 4.04 | mA | Sinking, dynamic |
| Analog inputs | | | | | | |
| | Input voltage range | -(VREFP-VREFM) | | VREFP+VREFM | V | (VINP-VINM) |
| $C_{INA}$ | Input capacitance [B] | 800 | | | fF | VINP (VINM) |
| $R_{INA}$ | Input resistance [B] | 500 | | | Ohm | |
| Digital inputs [C] | | | | | | |
| $V_{IH}$ | Input high voltage level | 1.4 | | | V | |
| $V_{IL}$ | Input low voltage level | | | 0.4 | V | |
| $C_{EN}$ | Input capacitance of «EN» | | | 96 | fF | |

## DEVICE PARAMETERS (continued)

| Symbol | Parameter | Min | Typ | Max | Unit | Conditions and comments |
|---|---|---|---|---|---|---|
| $C_{EN\_IEXT}$ | Input capacitance of «EN_IEXT» | | | 76 | fF | |
| $C_{CLK}$ | Input capacitance of «CLK» | | | 832 | fF | |
| $C_{NRES}$ | Input capacitance of «NRES» | | 7 | | pF | |
| $C_{MOSI}$ | Input capacitance of «MOSI» | | 136 | | fF | |
| $C_{NSS}$ | Input capacitance of «NSS» | | 148 | | fF | |
| $C_{SCLK}$ | Input capacitance of «SCLK» | | 355 | | fF | |
| $C_{RECLBR}$ | Input capacitance of «RECLBR» | | 178 | | fF | |
| Digital outputs | | | | | | |
| $V_{OH}$ | Output high voltage level | | | VDDD | V | |
| $V_{OL}$ | Output low voltage level | 0 | | | V | |
| $C_L$ | Load capacitance [C] | | 500 | | fF | Rising/falling edge is 2 ns |
| Current consumption [A] | | | | | | |
| Idda | Analog part | 27.4 | 33.8 | 44.2 | mA | $F_{CLK}$ = 20 MHz |
| Iddd | Digital part | 1.2 | 3.8 | 4.3 | mA | |
| Iddf | Clock module | 3.8 | 4.4 | 4.9 | mA | |
| Timing [C] | | | | | | |
| $F_{CLK}$ | Clock frequency | | | 20 | MHz | |
| $t_A$ | Aperture delay | 2.8 | 3.7 | 6.1 | ns | |
| $t_{CLK-CLKO}$ | CLK-CLKO delay | | 4.9 | | ns | |
| $t_L$ | Pipeline latency | | 7 | | periods | |
| SPI timing | | | | | | |
| $F_{SCLK}$ | SPI clock frequency | | | 20 | MHz | |
| $t_{SU}$ | Setup time of data after a rising edge of SPI clock | 25 | | | ns | |
| $t_{HD}$ | Hold time of data after a falling edge of SPI clock | 25 | | | ns | |
| $t_L$ | Leading time before the first SPI clock edge | 50 | | | ns | |
| $t_T$ | Trailing time after the last SPI clock edge | 50 | | | ns | |
| $t_I$ | Idling time between transfers | 50 | | | ns | |

*Notes:*

[A] Parameter is derived from measurements performed on 30 sampled devices from single wafer

[B] Input resistance and input capacitance represent on-resistance of input switch and total capacitance of the Hold capacitor

[C] Simulation results, 3-sigma statistical calculation

## PIN FUNCTIONAL DESCRIPTION

| Pin name | Description | Comments |
|---|---|---|
| EN | Enable ADC | Active level - high |
| VREFP | High reference voltage | |
| VINP | Analog input (+) | |
| VCM | Common-mode voltage | |
| VINM | Analog input (-) | |
| VREFM | Low reference voltage | |
| EN_IEXT | Enable external current source | Active level – high, disables internal biasing |
| CLK | Clock input | |
| NRES | Reset | Active level - low |
| MISO | Master input slave output | |
| MOSI | Master output slave input | |
| NSS | Slave select | Active level – low |
| SCLK | SPI input clock | |
| DC<11:0> | Digital output data <11:0> | |
| CLKO | Clock output | |
| RECLBR | Recalibration | Activates at falling edge |
| CLBR_DONE | “End of calibration” output signal | Active level - high |
| IMEAS | Current measurement output | |
| IEXT | External current input | |
| VDDF | Clock module power supply | Typical value: 5 V |
| VSSF | Clock module ground | |
| VDDA | Analog power supply | Typical value: 5 V |
| VSSA | Analog ground | |
| VDDD | Digital power supply | Typical value: 1.8 V |
| GNDD | Digital ground | |
| SHIELD | Shield (ground) | |

## DEVICE OPERATION

This analog-to-digital converter has pipelined architecture with internal Sample and Hold circuit. The input equivalent circuit is given in Figure 1.

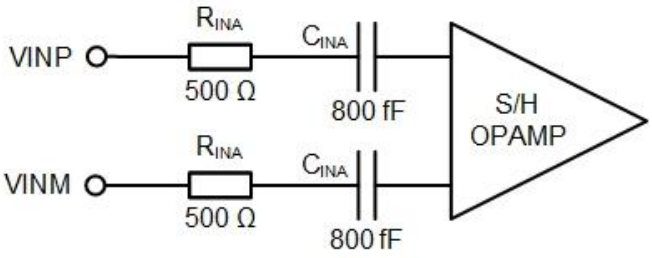


*Figure 1. Equivalent analog input circuit (during sampling phase)*

Input signal source output resistance must be also considered for proper sampling as shown in Figure 2.

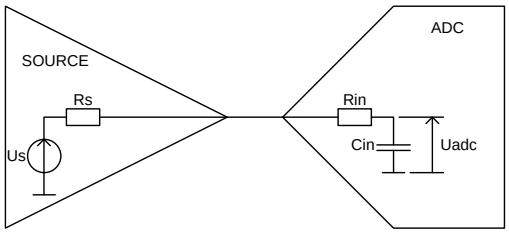


*Figure 2. Equivalent electrical circuit of signal source and ADC*

The time constant of the circuit, to achieve an error less than 1/16LSB, is given by:

$$TC_{1/16LSB} = (R_S + R_{IN}) \times C_{IN} \times \ln 2^{(N+4)}$$

Where N is the resolution of the converter (in this case N=12).

The required input time constant must be small enough to be within the given ADC analog input sampling time. The acquisition for $TC_{1/16LSB}$ should be used for calculation of maximum value of external driving source resistance to provide a desired ADC conversion accuracy.

The pipeline conversion core includes eight 1.5-bit stages and one 4-bit flash ADC. Every 1.5-bit stage receives an analog signal from the previous stage and produces output data that is sent further to the digital error-correction module.

S/H and every subsequent conversion stage have additional DACs for calibration of offset and gain of each stage. These DACs are controlled with stored register values. The process of data writing into the registers is performed by calibration state machine or by a user through SPI. In case of low «NSS» signal a user performs the process of data writing into all internal registers (not only calibration registers), otherwise the calibration is carried out automatically. During automatic calibration several iterations (256 iterations by default) with averaging are performed for the binary search of tuning coefficients. Approximate calibration time is calculated as follows:

$$t_{cal} \approx n_{iter} \times T_{CLK} \times n_{c/iter}$$

Where $n_{iter}$ is the number of iterations and $n_{c/iter}$ is the number of clock cycles per iteration.

At typical settings, the approximate time of calibration is 12.8 ms (~1000 clock cycles per iteration at 50 ns clock period). If recalibration is needed (for instance due to change in temperature), it can

be started by a pulse to «RECLBR». All the data of internal registers can be turned into default values via asserting «NRES» low.

Output data is valid for reading during falling edge of «CLKO». Latency of ADC is 7 input clock frequency periods. Sampling of the input signal is performed at the rising edge of «CLK» signal + aperture delay $t_A$ (at the end of the sampling phase and the beginning of the hold phase).

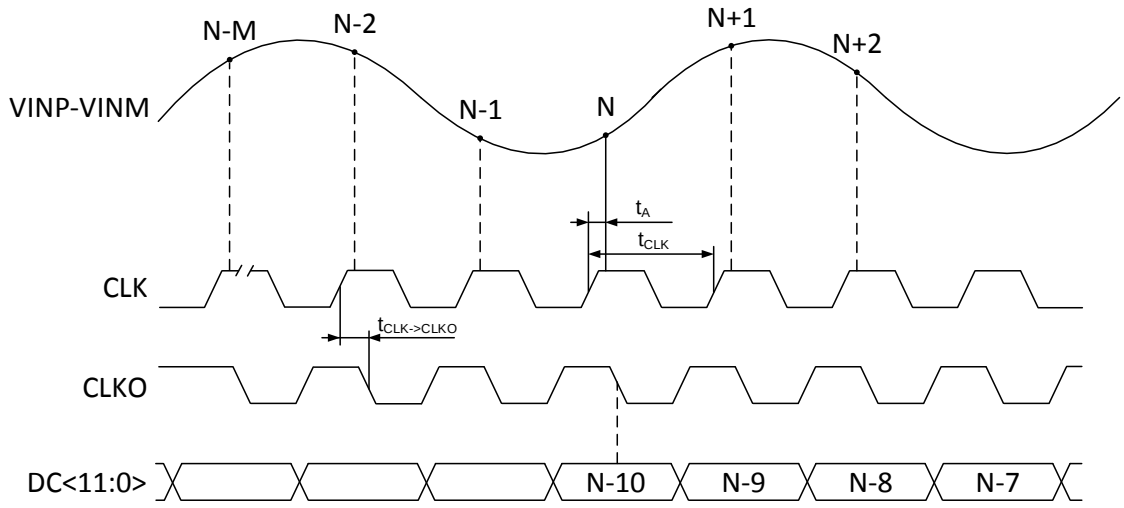


*Figure 3. Timing diagram*

Input signal charges the hold capacitor in Sample-and-Hold circuit during sample phase (when «CLK» is low) and S/H holds the value of the input signal at the end of the sample phase (at the rising edge of «CLK» + $t_A$).

Output data type is fully parallel.

The integrated SPI allows user to configure the ADC: biasing current, calibration coefficients of each stage, number of calibration iterations, delay between offset and gain calibrations.

The ADC's SPI operates as a slave relative to a user.

For reading or writing operation 16 bits should be transmitted to «MOSI». The first 8 bits is address (MSB defines reading if it is low and writing if it is high), and following 8 bits is data. The data in the SPI is latched at the falling edge of «SCLK». The transmitted data format is «LSB - first». Therefore, the reading/writing bit is the 8$^{th}$ bit in this chain.

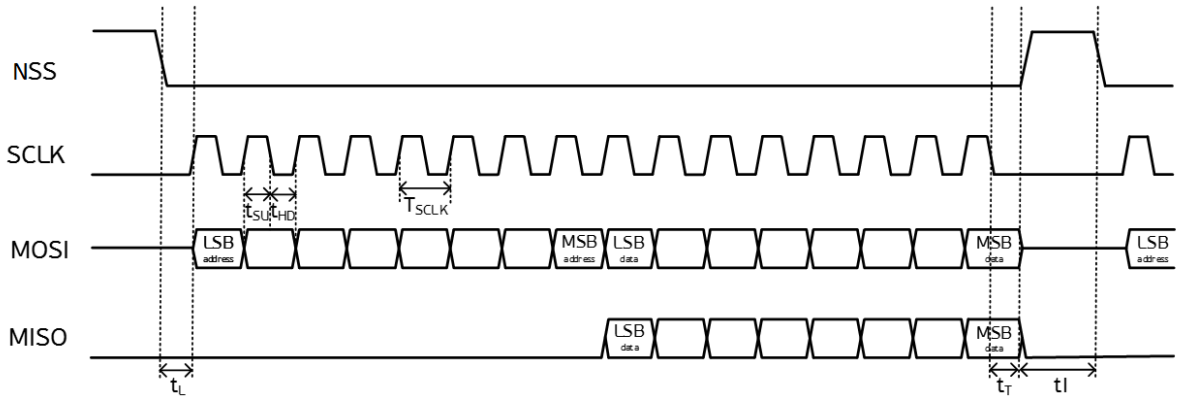


*Figure 4. SPI timing diagram*

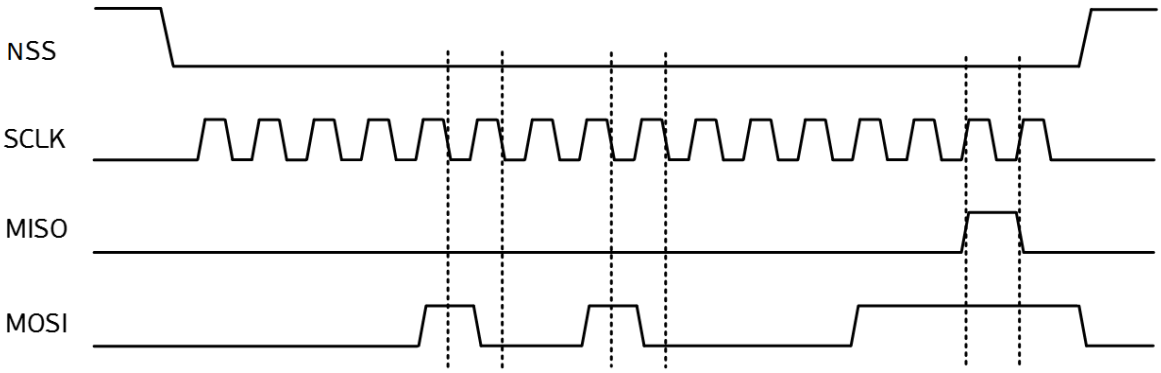


*Figure 5. SPI example*

On figure 5 there is an example of writing the data F0 into a gain tuning coefficient for the S/H register (0x90). Simultaneously default data of the register is being transmitted from the ADC to «MISO».

## MEMORY MAP REGISTERS TABLE

| Address | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | Description |
|---|---|---|---|---|---|---|---|---|---|
| 0x00 | - | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Gain tuning coefficient for 1st stage (reading); default value: 40 |
| 0x80 | - | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Gain tuning coefficient for 1st stage (writing) |
| 0x01 | Sign | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Offset tuning coefficient for 1st stage (reading); default value: 0 |
| 0x81 | Sign | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Offset tuning coefficient for 1st stage (writing) |
| 0x02 | - | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Gain tuning coefficient for 2nd stage (reading); default value: 40 |
| 0x82 | - | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Gain tuning coefficient for 2nd stage (writing) |
| 0x03 | Sign | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Offset tuning coefficient for 2nd stage (reading); default value: 0 |
| 0x83 | Sign | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Offset tuning coefficient for 2nd stage (writing) |
| 0x04 | - | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Gain tuning coefficient for 3rd stage (reading); default value: 40 |
| 0x84 | - | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Gain tuning coefficient for 3rd stage (writing) |
| 0x05 | Sign | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Offset tuning coefficient for 3rd stage (reading); default value: 0 |
| 0x85 | Sign | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Offset tuning coefficient for 3rd stage (writing) |
| 0x06 | - | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Gain tuning coefficient for 4th stage (reading); default value: 40 |
| 0x86 | - | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Gain tuning coefficient for 4th stage (writing) |
| 0x07 | Sign | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Offset tuning coefficient for 4th stage (reading); default value: 0 |
| 0x87 | Sign | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Offset tuning coefficient for 4th stage (writing) |
| 0x08 | - | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Gain tuning coefficient for 5th stage (reading); default value: 40 |
| 0x88 | - | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Gain tuning coefficient for 5th stage (writing) |
| 0x09 | Sign | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Offset tuning coefficient for 5th stage (reading); default value: 0 |
| 0x89 | Sign | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Offset tuning coefficient for 5th stage (writing) |
| 0x0A | - | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Gain tuning coefficient for 6th stage (reading); default value: 40 |
| 0x8A | - | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Gain tuning coefficient for 6th stage (writing) |
| 0x0B | Sign | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Offset tuning coefficient for 6th stage (reading); default value: 0 |
| 0x8B | Sign | $6^{th}$ bit | $5^{th}$ bit | $4^{th}$ bit | $3^{rd}$ bit | $2^{nd}$ bit | $1^{st}$ bit | $0^{th}$ bit | Offset tuning coefficient for 6th stage (writing) |

## MEMORY MAP REGISTERS TABLE (continued)

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 0x0C | - | 6th bit | 5th bit | 4th bit | 3rd bit | 2nd bit | 1st bit | 0th bit | Gain tuning coefficient for 7th stage (reading); default value: 40 |
| 0x8C | - | 6th bit | 5th bit | 4th bit | 3rd bit | 2nd bit | 1st bit | 0th bit | Gain tuning coefficient for 7th stage (writing) |
| 0x0D | Sign | 6th bit | 5th bit | 4th bit | 3rd bit | 2nd bit | 1st bit | 0th bit | Offset tuning coefficient for 7th stage (reading); default value: 0 |
| 0x8D | Sign | 6th bit | 5th bit | 4th bit | 3rd bit | 2nd bit | 1st bit | 0th bit | Offset tuning coefficient for 7th stage (writing) |
| 0x0E | - | 6th bit | 5th bit | 4th bit | 3rd bit | 2nd bit | 1st bit | 0th bit | Gain tuning coefficient for 8th stage (reading); default value: 40 |
| 0x8E | - | 6th bit | 5th bit | 4th bit | 3rd bit | 2nd bit | 1st bit | 0th bit | Gain tuning coefficient for 8th stage (writing) |
| 0x0F | Sign | 6th bit | 5th bit | 4th bit | 3rd bit | 2nd bit | 1st bit | 0th bit | Offset tuning coefficient for 8th stage (reading); default value: 0 |
| 0x8F | Sign | 6th bit | 5th bit | 4th bit | 3rd bit | 2nd bit | 1st bit | 0th bit | Offset tuning coefficient for 8th stage (writing) |
| 0x10 | - | 6th bit | 5th bit | 4th bit | 3rd bit | 2nd bit | 1st bit | 0th bit | Gain tuning coefficient for S/H (reading); default value: 40 |
| 0x90 | - | 6th bit | 5th bit | 4th bit | 3rd bit | 2nd bit | 1st bit | 0th bit | Gain tuning coefficient for S/H (writing) |
| 0x11 | Sign | 6th bit | 5th bit | 4th bit | 3rd bit | 2nd bit | 1st bit | 0th bit | Offset tuning coefficient for S/H (reading); default value: 0 |
| 0x91 | Sign | 6th bit | 5th bit | 4th bit | 3rd bit | 2nd bit | 1st bit | 0th bit | Offset tuning coefficient for S/H (writing) |
| 0x28 | - | - | - | - | 3rd bit | 2nd bit | 1st bit | 0th bit | Internal current source settings (reading); default value: 8 |
| 0xA8 | - | - | - | - | 3rd bit | 2nd bit | 1st bit | 0th bit | Internal current source settings (writing) |
| 0x20 | 7th bit | 6th bit | 5th bit | 4th bit | 3rd bit | 2nd bit | 1st bit | 0th bit | Number of calibration iterations settings (reading); default value: 2F |
| 0xA0 | 7th bit | 6th bit | 5th bit | 4th bit | 3rd bit | 2nd bit | 1st bit | 0th bit | Number of calibration iterations settings (writing) |
| 0x22 | 7th bit | 6th bit | 5th bit | 4th bit | 3rd bit | 2nd bit | 1st bit | 0th bit | Settings for delay between calibration states (reading); default value: 2 |
| 0xA2 | 7th bit | 6th bit | 5th bit | 4th bit | 3rd bit | 2nd bit | 1st bit | 0th bit | Settings for delay between calibration states (writing) |

## INTERNAL CURRENT SOURCE

The implemented current source is a general purpose current source. It is supplied from VDDA source for operation and has one output that drives typical current of 60 uA at typical combination "1000" for trimming inputs B<3:0>.

Internal current source output current (VDDA = 5 V, T = 27°C)

| Code | Output current, uA |
|---|---|
| B<3:0>=0000 | 20.0 |
| B<3:0>=0001 | 25.0 |
| B<3:0>=0010 | 30.0 |
| B<3:0>=0011 | 35.0 |
| B<3:0>=0100 | 39.9 |
| B<3:0>=0101 | 44.9 |
| B<3:0>=0110 | 49.9 |
| B<3:0>=0111 | 54.8 |
| B<3:0>=1000 | 59.7 |
| B<3:0>=1001 | 64.7 |
| B<3:0>=1010 | 69.6 |
| B<3:0>=1011 | 74.5 |
| B<3:0>=1100 | 79.4 |
| B<3:0>=1101 | 84.3 |
| B<3:0>=1110 | 89.2 |
| B<3:0>=1111 | 94.1 |

External current for biasing must be in the same range as internal current source output, that is from 20 uA to 94 uA.

## REQUIREMENTS FOR POWER SUPPLY AND GROUND NETS

Analog and digital power supplies wiring should be split, because the analog blocks require isolation from digital power supply noise.

## REQUIREMENTS FOR EXTERNAL COMPONENTS

Analog inputs need a differential input buffer that should meet the requirements to analog inputs: analog inputs capacitance and sample rate.

Input buffer SNR should be more than 80 dB at desired input frequency (for example, 3 MHz).

Reference inputs also require buffers meeting the requirements to reference inputs according to the Device Parameters table.

Analog input buffer should be placed as close as possible to the analog inputs. The length of analog inputs paths («VINP»/«VINM») should be equal.

The reference input buffers are necessary. They should be placed as close as possible to the reference inputs («VREFP», «VCM», «VREFM»).

It is recommended to use 10 uF tantalum (or 100 uF low ESR electrolytic) capacitor in parallel with 100 nF ceramic capacitor as external capacitors for supply and ground nets. Keep the PCB tracks as short as possible to ground and to capacitors.

## CRITICAL APPLICATION NOTES

«VREFP», «VCM», «VREFM», «VINP» and «VINM» are highly sensitive analog signals: any noise at these inputs or cross-talks from high frequency signals to these pins can alter overall ADC accuracy. Thus, it is recommended to shield these signals with analog ground, and fast-switching signals should never be run near (under/over) metal lines leading to these input pins.

Although «VDDF» and «VDDA» are of the same voltage, their wiring should be split, because «VDDF» is a supply for clock buffers and it is considered rather noisy.

It is recommended to connect «SHIELD» with «VSSA».

## TYPICAL PERFORMANCE CHARACTERISTICS

The figures are obtained by measurements. Due to the inevitable lot-to-lot tolerances, the values given below may differ from typical values in the table above.

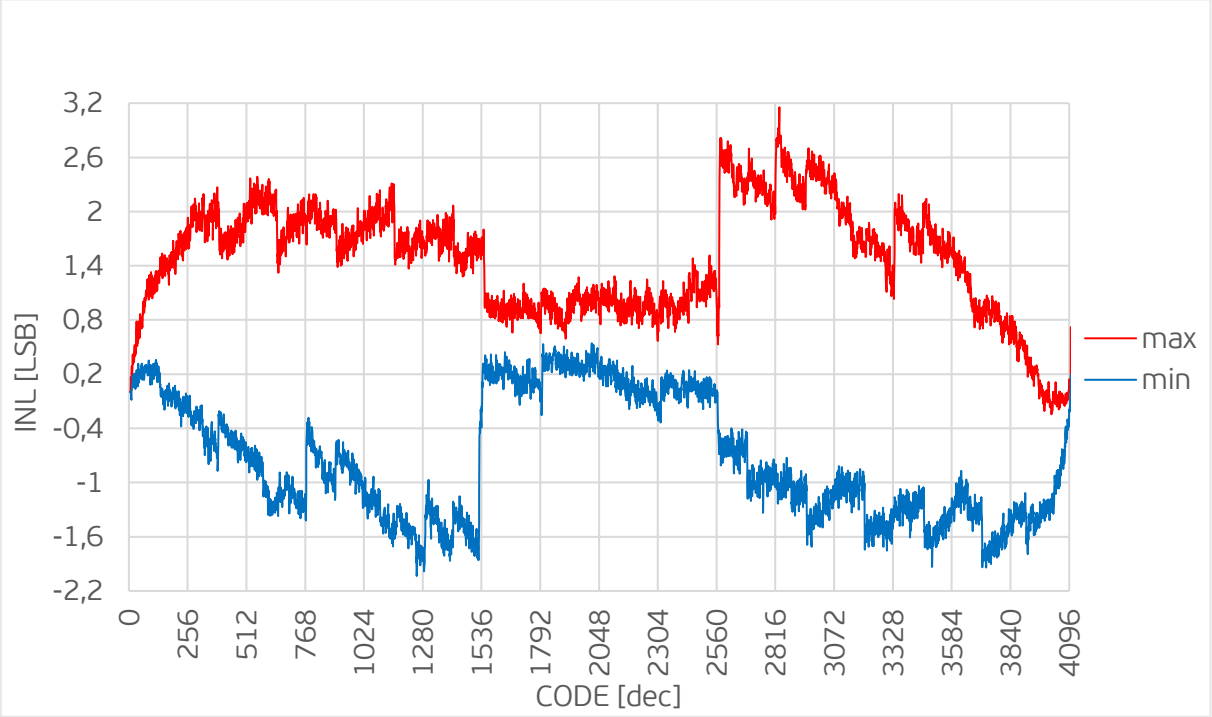


*Figure 6. Minimal and maximal INL vs output code at typical conditions (VDDA = VREFP = 5 V; VDDD = 1.8 V; T = 27°C; $F_{CLK}$ = 20 MHz; $F_{in}$ = 1.3 MHz)*

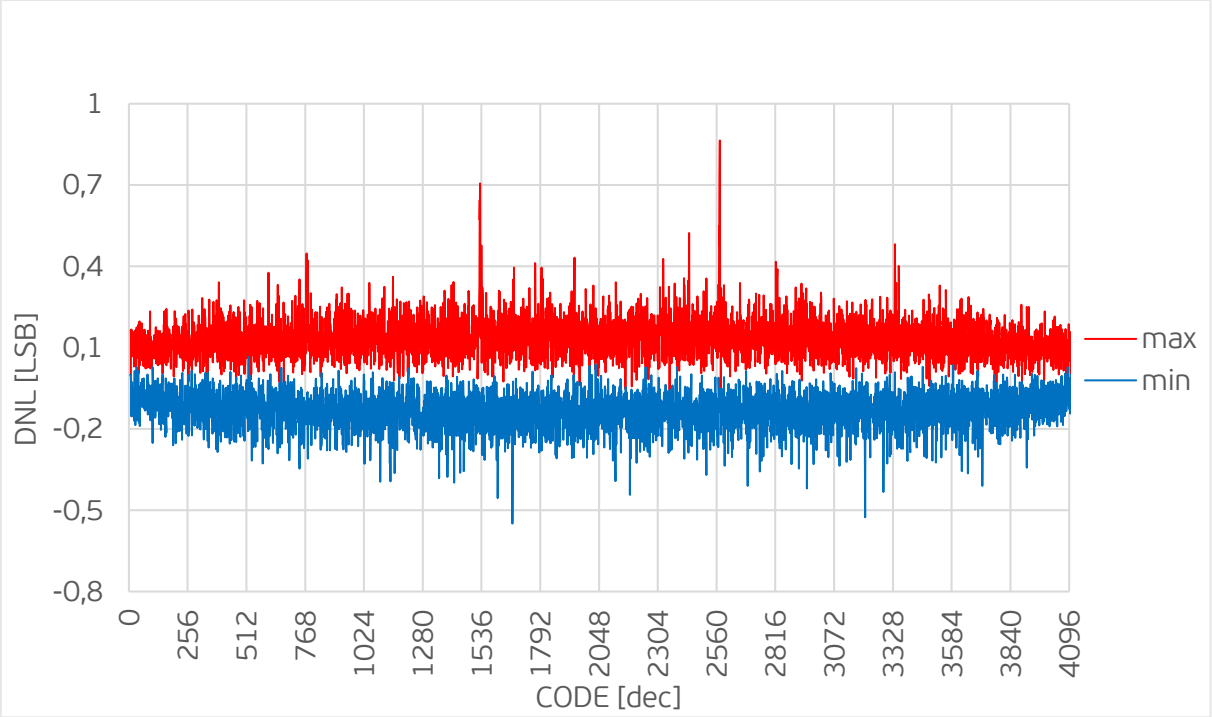


*Figure 7. Minimal and maximal DNL vs output code at typical conditions (VDDA = VREFP = 5 V; VDDD = 1.8 V; T = 27°C; $F_{CLK}$ = 20 MHz; $F_{in}$ = 1.3 MHz)*

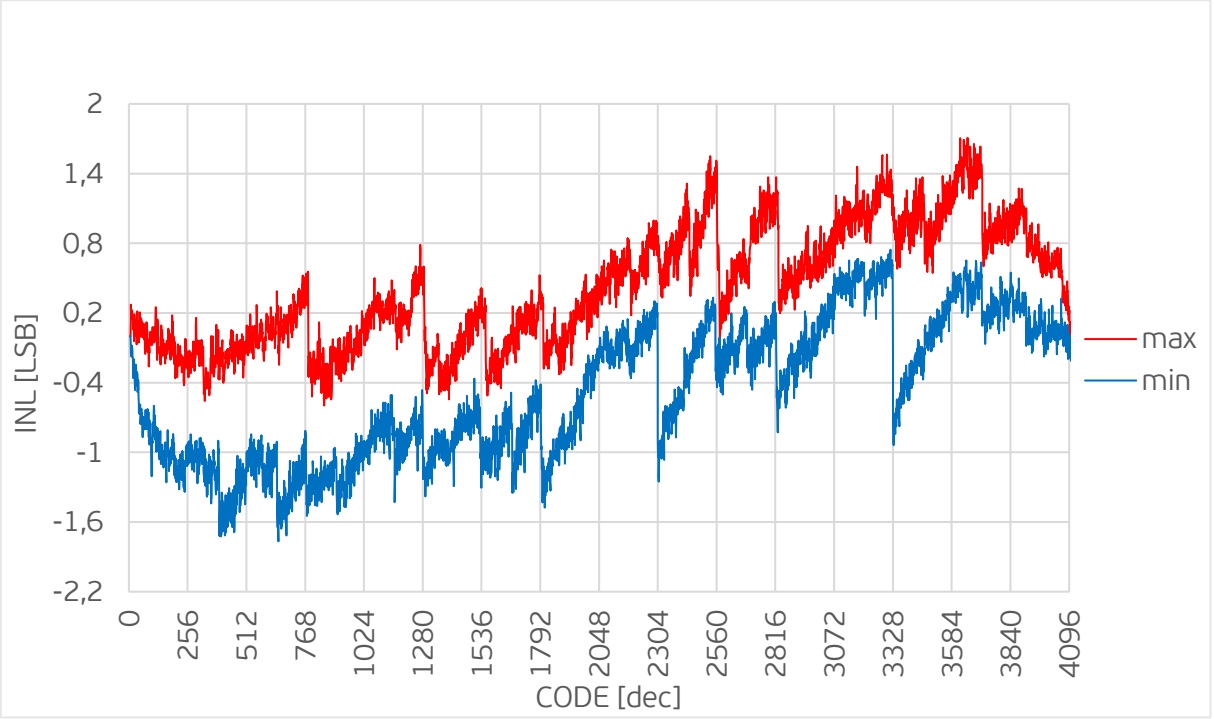


*Figure 8. Minimal and maximal INL vs output code at high temperatures (VDDA = VREFP = 4.5 V; VDDD = 1.62 V; T = 150°C; $F_{CLK}$ = 20 MHz; $F_{in}$ = 1.3 MHz)*

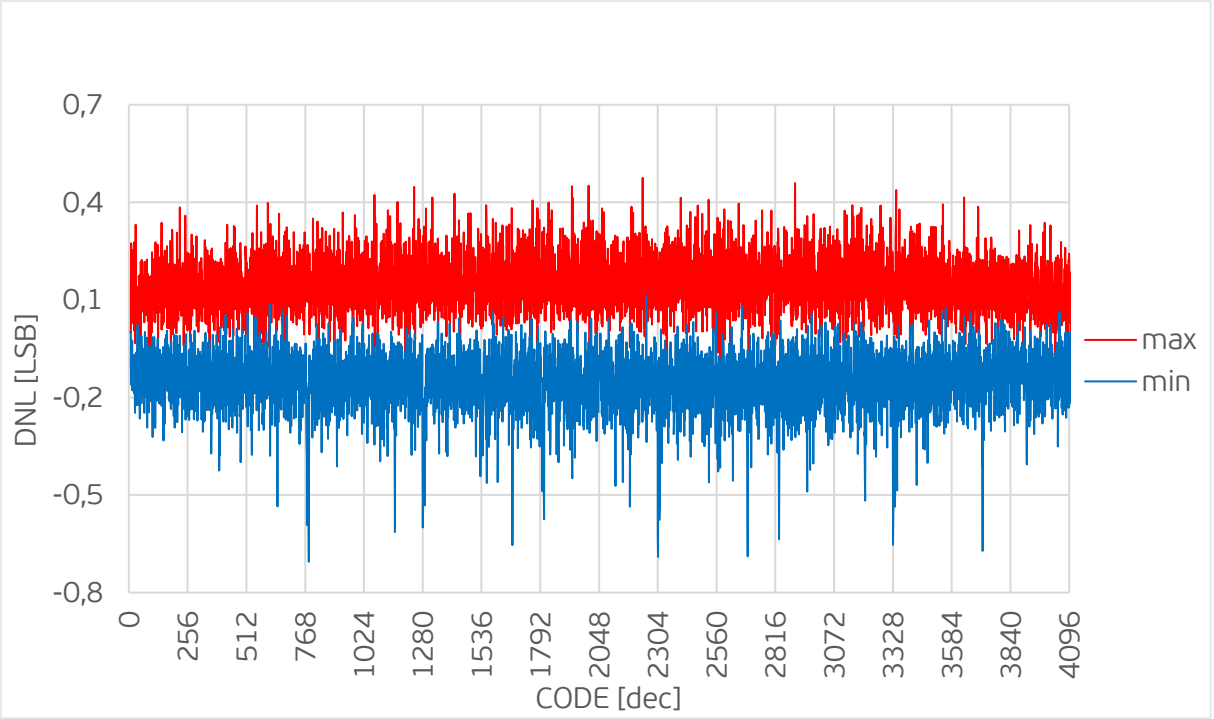


*Figure 9. Minimal and maximal DNL vs output code at high temperatures (VDDA = VREFP = 4.5 V; VDDD = 1.62 V; T = 150°C; $F_{CLK}$ = 20 MHz; $F_{in}$ = 1.3 MHz)*

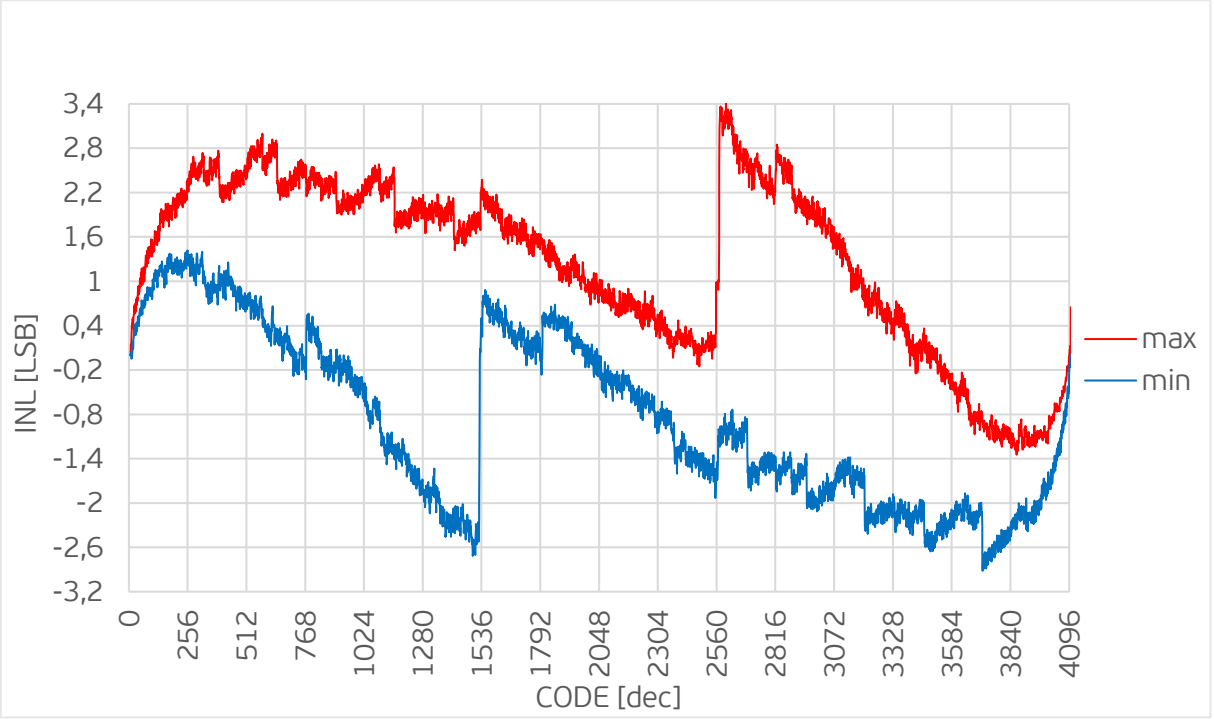


*Figure 10. Minimal and maximal INL vs output code at low temperatures (VDDA = VREFP = 5.5 V; VDDD = 1.98 V; T = -40°C; $F_{CLK}$ = 20 MHz; $F_{in}$ = 1.3 MHz)*

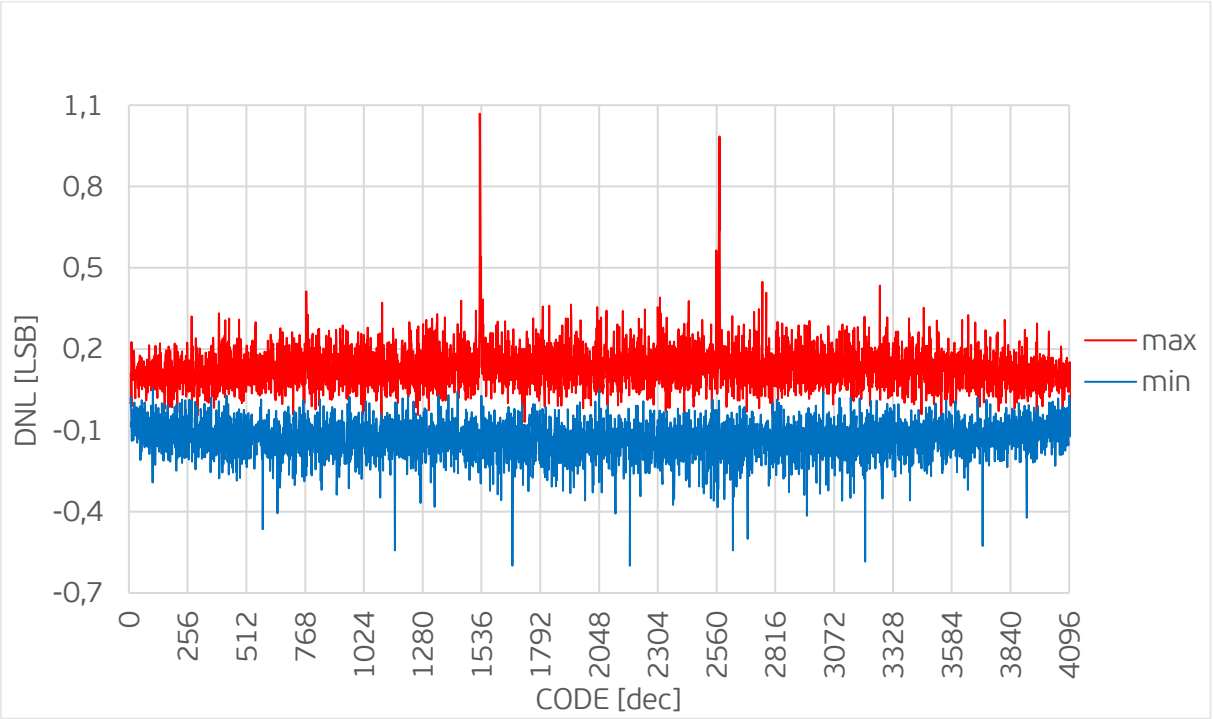


*Figure 11. Minimal and maximal DNL vs output code at low temperatures (VDDA = VREFP = 5.5 V; VDDD = 1.98 V; T = -40°C; $F_{CLK}$ = 20 MHz; $F_{in}$ = 1.3 MHz)*